REMARKS

Restriction Requirement

With respect to the previous Restriction Requirement, non-elected claims 58-62 and 75-89 have been canceled from the present application. Applicant reserves the right to file a separate divisional application with the canceled claims.

Claim Rejections Under 35 USC §102 and 35 USC §103

Claims 63, 65-66, 90, 92-94, 96, 98-99 and 102 have been rejected under 35 USC 102(b) as being anticipated by Bhatt et al. (US Patent No. 5,487,218).

Claims 63, 65-66, 90, 92-93, 96, 98, and 101 have been rejected under 35 USC 102(b) as being anticipated by Geldermans et al. (4,617,730).

Claims 63, 65-66, 90, 92, 94, 96, 98-99, and 101 have been rejected under 35 USC 102(b) as being anticipated by Vafi et al. (5,474,458).

Claims 63, 65, 90-91, 96 and 100 have been rejected under 35 USC 102(b) as being anticipated by Capps et al. (US Patent No. 5,432,999).

Claims 63-66, 90, 92, 94-99 and 101 have been rejected under 35 USC 102(a) as being anticipated by Tomura et al (US Patent No. 5,640,051).

Claims 64, 95 and 97 have been rejected under 35 USC 103(a) as being unpatentable over each of Bhatt et al. (US Patent No. 5,487,218) Geldermans et al. (US Patent No. 4,617,730 and Vafi et al. (US Patent No. 5,474,458) in combination with Iwasaki (US Patent No. 5,834,848).

The rejections under 35 USC §102(b) and 35 USC §103(a) are traversed for the reasons to follow.

Summary of the Invention

Claims 63-66 and 90-101 are directed to the package 130 shown in Figure 8. The package 130 includes a semiconductor die 20D, an interconnect 10C attached to the die 20D, and an underfill layer 128 between the die 20D and the interconnect 10C. The interconnect 10C includes contacts 32F which comprise recesses and conductive layers bonded to bumped external contacts 18 on the die. The interconnect 10C also includes conductive members 34C comprising openings in the substrate 10C and the contacts 32F, containing a conductive material, such as a solder, a metal or a conductive polymer. In addition, the interconnect 10C includes external contact balls 38C in electrical communication with the conductive members 34C.

35 USC §102 Rejections Of Claims 63, 65-66, 90, 92-94, 96, 98-99 and 102 Over Bhatt et al.

A proper 35 USC §102 rejection requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. In addition, the reference must be enabling and describe the applicant's claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention. In re David C. Paulsen, 30 F.3d 1475, 31 USPQ 2d (BNA) 1671, (U.S. App 1994).

Each of the independent claims has been amended to include additional limitations that define features which distinguish the presently claimed semiconductor component from Bhatt et al. and the prior art.

One distinguishing feature is that the conductive members 34C (Figure 8) include openings 30 (Figure 1B) which are formed through both the conductive layers 26 (Figure 1B) for the contacts 32F (Figure 8), and the substrate 10C (Figure 8) of the interconnect 40C (Figure

8). In the illustrative embodiment the openings 30 (Figure 1B) are formed using a laser machining process. This permits the openings 30 (Figure 1B) for the conductive members 34C (Figure 8) to be small and accurately formed. In addition, alignment of the contacts 32F (Figure 8) with the conductive members 34C (Figure 8) is insured, because a single opening forms the conductive members 34C (Figure 8), and electrically connects the conductive members 34C to the contacts 32F (Figure 8).

With respect to Bhatt et al., this reference does not teach or suggest an interconnect having conductive members with openings that extend through both contacts, and a substrate of the interconnect. Specifically, Bhatt et al. teaches at column 3, lines 23-26: "Plated through hole 7b is filled with fill composition 11, and extends through the subcomposite 3 up to the optional film redistribution layer 5, when present, where it terminates in a conductive copper cap 13." However, there is no suggestion of the through hole 7b being a continuous opening which extends through both the redistribution layer 5 and the subcomposite 3.

Independent claim 63 has been amended to state that the conductive member includes "an opening extending through the conductive layer and the interconnect". Independent claims 90 and 96 have been amended with similar recitations. Antecedent basis for these recitations is contained on page 11, lines 20-24 of the specification. This feature in combination with the other claimed features is submitted to make all of the claims novel and unobvious over Bhatt et al., and the additional cited art as well.

A second distinguishing feature is that the configuration of the conductive members 34C (Figure 8) and the contacts 32F (Figure 8) of the interconnect 40C (Figure

8) permits a chip scale package 130 to be fabricated. In contrast, Bhatt et al. is directed to a printed circuit board 1 having an outline that is much larger than the chips. In order to emphasize this feature, independent claims 90 and 96 have been amended to state that the interconnect has "a chip scale outline". Antecedent basis for this recitation is contained on page 27, lines 37-38 of the specification.

A third distinguishing feature recited in amended dependent claim 65 is that the conductive material can "comprise solder substantially filling the opening." Antecedent basis for this recitation is contained on page 12, lines 26-32 of the specification. In Bhatt et al. plated through holes 7b are filled with a fill composition 11. In the presently claimed package, the solder provides a high electrical conductivity, and an easily bondable material.

A fourth distinguishing feature recited in amended dependent claim 66 is that the contacts 32F (Figure 8) can "include a penetrating member configured to penetrate the bumped contact". Antecedent basis for this recitation is contained on page 5, lines 14-17 of the specification. In addition, the penetrating members 22 are shown in Figure 3A. The penetrating members function to penetrate oxide layers on the external contacts 18 to insure low resistance electrical connections.

In view of these features the amended claims are submitted to be both novel and unobvious over Bhatt et al.

35 USC §102 Rejections Of Claims 63, 65-66, 90, 92-93, 96, 98 and 101 Over Geldermans et al.

Amended independent claims 63, 90 and 96 are submitted to patentably distinguish the claimed package from Geldermans et al. for essentially the same reasons as stated above for Bhatt et al. In particular, as shown in Figure 6 of Geldermans et al., via holes 29 do not extend through metallization layers 18 or contacts 19. In addition, Geldermans et al. is directed to a multi chip interposer 24 (Figure 2) that does not have a chip scale outline. Further, contact pads 31 (Figure 8) in Geldermans et al. comprise Cu rather than solder (column 5, lines 45-50), and the contacts 19 (Figure 1) do not include penetrating members.

35 USC §102 Rejections Of Claims 63, 65-66, 90, 92, 94, 96, 98-99 and 101 Over Vafi et al.

Amended independent claims 63, 90 and 96 are submitted to patentably distinguish the claimed package from Vafi et al. for essentially the same reasons as stated above for Bhatt et al. In particular, as shown in Figure 1 of Vafi et al., conductive vias 7 do not extend through conductive pads 8 and 9. In addition, the outline of the interposer 10 (Figure 3) and the major substrate 3 (Figure 3) appear to be much larger than the chip 1. Still further, conductive vias 7 (Figure 1) do not comprise solder, and the conductive pads 8 and 9 (Figure 1) do not include penetrating members.

35 USC §102 Rejections Of Claims 63, 65, 90-91, 96 and 100 Over Capps et al.

Amended independent claims 63, 90 and 96 are submitted to patentably distinguish the claimed package from Capps et al. for essentially the same reasons as stated above for Bhatt et al. In particular, as shown in Figure 9 of Capps et al., the openings for conductive posts 26, 28 do not extend through conductive pads 42. In addition, the conductive posts 26, 28 are preferably a refractory metal (column 6, line 20) rather than solder, and the conductive pads 42 do not include penetrating members.

35 USC §102 Rejections Of Claims 63-66, 90, 92, 94-99 and 101 Over Tomura et al.

Amended independent claims 63, 90 and 96 are submitted to patentably distinguish the claimed package from Tomura et al. for essentially the same reasons as stated above for Bhatt et al. In particular, as shown in Figure 2 of Tomura et al., the openings 2 for conductive members 3 do not extend through the contacts 6. In addition, the conductive members 3 do not comprise solder, and the contacts 6 do not include penetrating members.

35 USC §103 Rejections Of Claims 64, 95 and 97 Over Bhatt et al., Geldermans et al and Vafi et al. in combination with Iwasaki

Claims 64, 95 and 97 rejected under 35 USC §103 include the recitation of an underfill layer. Iwasaki was cited as teaching an underfill layer. However, Bhatt et al., Geldermans and Vafi et al. in combination, do not teach the above features recited in independent claims 63, 90 and 96. Accordingly, claims 64, 95 and 97 are submitted to be unobvious over the cited combination of art.

Conclusion

In view of the amendments and arguments, favorable consideration and allowance of claims 63-66 and 90-101 is requested. Should any issues remain, the Examiner is requested to contact the undersigned by telephone.

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